UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,106	08/14/2001	Stephen E. Jones	149148001US1	9880

25096 7590 12/11/2007

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/930,106	JONES, STEPHEN E.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27,29-34,36,37,39-44,47,48 and 50-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,26,27 and 29-34* is/are allowed.

6)☒ Claim(s) *5-25,36,37,39-44,47,48 and 50-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Withdrawn Rejections

1. Applicant, via amendment, has overcome the rejection of claims 26-29, 31-32, 35-39, 41-42, 45, 47-50, 52-53 and 56 under 35 U.S.C. 112, first paragraph. The rejection has been respectfully withdrawn.

2. Applicant, via amendment, has overcome the rejection of claims 1-17 and 26-45 rejected under 35 U.S.C. 112, second paragraph. The rejection has been respectfully withdrawn.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 18-25, 46 and 54-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Wooten (U.S. Patent No. 5,832, 299) herein referred to as Wooten'299.

4. Referring to claim 18, Wooten'299 discloses, as claimed, a computer-readable medium containing instructions for an SMI routine that allows execution of code that resides in physical address space above address 0x100000, by a

method comprising: saving state (such as EIP, and EFLAGS, see Col. 15, lines 36-41, or Col. 16, lines 38-42) of the processor; switching the processor to protected mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E); and before returning from the interrupt, executing code that resides in physical address space above address 0x100000 (this is the existing feature when the Wooten'299's system is based on an Intel Pentium processor (as indicated in Col. 4, lines 29-30); code is certainly executed above 0x100000 in a 4GB address space; see col. 11, lines 1-5).

Note that the claim merely requires the instructions allow these actions, they do not require that the actions actually take place

5. As to claim 19, Wooten'299 also discloses: after executing the code, restoring the saved state of the processor and returning from the SMI (the saved state must be restored if the mode is transparent to the other code; see col. 5, lines 55-60).

6. As to claim 20, Wooten'299 also discloses the code is executed using a global descriptor table that is different from the global descriptor table in use when the SMI occurred (see col. 11, lines 21-38).

7. As to claim 21, Wooten'299 also discloses: the computer system is based on an Intel Pentium processor (as indicated in Col. 4, lines 29-30).

8. As to claim 22, Wooten'299 also discloses: the method of claim 5 wherein the executing executes 32-bit (note the Wooten'299's protected mode is a flat 32 bit model).

9. As to claim 23, Wooten'299 also discloses: the computer-readable medium of claim 18 wherein the instructions are loaded into system management memory (inside such as memory unit 102, see Fig. 1a) by a BIOS.

10. As to claim 24, Wooten'299 also discloses: the computer-readable medium of claim 18 wherein the code is loaded into memory from a ROM (110 see Fig. 1A).

11. As to claim 25, Wooten'299 also discloses: the computer-readable medium of claim 18 wherein the code is loaded into memory from a flash ROM (110 see Fig. 1A, note the ROM can be a flash type).

12. As to claim 46, Wooten'299 also discloses the method is performed in response to the receipt of an SMI by a processor (Virtual System Mode Interrupt, see Col. 15, lines 60-61. Note the Wooten'299's Virtual System Mode is best reasonably and broadly interpreted as the claimed System Management Mode).

13. As to claim 54, Wooten'299 also discloses an electronic circuit is the source of the SMI (an interrupt is generated by a circuit).

14. As to claim 55, Wooten'299 also discloses returning from the interrupt by executing an RSM instruction (any means for returning from the SMI could be considered a return from system mode instruction).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 5-17, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wooten'299 in view of Russell et al. (U.S. Patent No. 6,751,737) herein referred to as Russell.

17. Referring to claim 5, Wooten'299 discloses, as claimed, a method in a computer system for executing code during a system management mode interrupt (Virtual System Mode Interrupt, see Col. 15, lines 60-61), the method

comprising: upon occurrence of a system management mode interrupt (Virtual System Mode Interrupt, see Col. 15, lines 60-61), switching the computer system to another mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E); executing code (the code running in the Wooten'299's protected mode) that uses a global descriptor table (segment descriptor 402, see Fig. 4) that is different from the global descriptor table in use when the system management mode interrupt occurred (note the segment descriptor 402, see Fig. 4, will be different when referring to different segments at the different state of the Wooten'299's system before and after interrupt occurrence).

Wooten'299 does not expressly disclose a global descriptor table register or replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table.

Russell teaches disclose a global descriptor table register (MVM Context Register 128; see fig. 1) or replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table (see col. 8, lines 55-60).

For combination and motivation, see above regarding claim 1.

18. As to claim 9, Wooten'299 also discloses: the 32-bit code is an operating system kernel for loading and running programs (since in the Wooten'299's system, the operating system kernel certainly comprises programs for an

interrupt handling; and loading and running are the certain operations therein) during the occurrence of the system management mode interrupt.

As to claims 3 and 10, Wooten'299 also discloses: the programs are Windows Portable Executable programs (since Windows NT operating system is intended to be used in the Wooten'299's system).

19. As to claim 11 Wooten'299 also discloses: the computer system is based on an Intel Pentium processor (as indicated in Col. 4, lines 29-30).

20. As to claim 6, Wooten'299 also discloses: the method of claim 5 including upon completion of the execution of the code, returning (by IRET instruction, see Col. 18, lines 33-37) from the occurrence of the system management mode interrupt.

21. As to claim 7, Wooten'299 also discloses: the method of claim 5 including: saving state (such as EIP, and EFLAGS, see Col. 15, lines 36-41, or Col. 16, lines 38-42) of the computer system; and upon completion of the execution of the 32-bit code, restoring (see Col. 18, lines 27-37, regarding restoring the EIP register and the EFLAGS register) the saved state of the computer system; and returning (by IRET instruction, see Col. 18, lines 33-37) restoring from the occurrence of the interrupt.

22. As to claim 8 Wooten'299 also discloses: the method of claim 5 wherein the executing executes 32-bit (note the Wooten'299's protected mode is a flat 32 bit model).

23. As to claim 12, Wooten'299 also discloses: the computer system is based on an Intel-compatible processor (as indicated in Col: 4, lines 29-30).

24. As to claim 13, as bets understood, Wooten'299 also discloses: the method of claim 5 wherein the programs are selected from the group consisting of a remote console program, a remote boot program, a remote diagnostics program, a remote restart program, and a debugging program (see Col. 19, lines 15-67 and Col. 29, regarding the instruction set formats such as VMOVS; VTOP EAX, memory; and PROBER suitable for the set forth programs).

25. As to claim 14, Wooten'299 also discloses: the method of claim 5 wherein the other mode is protected mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E).

26. As to claim 15, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the code executes transparently (see Col. 17, lines 39-45) to the foreground operating system.

27. As to claim 16, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the code executes even if the foreground operating system has crashed or stopped (see Col. 15, lines 9-67, and Col. 16, regarding the interrupts/exceptions).

28. As to claim 17, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the code executes when the foreground operating system crashes or stops (see Col. 15, lines 9-67, and Col. 16, regarding the interrupts/exceptions).

29. Claims 43 and 44 recite equivalent limitations as claims 54 and 55. These claims are rejected for the same reasons.

30. Claims 47-53 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wooten'299 in view of common knowledge in the art.

31. As to claim 47, Examiner asserts that it was common knowledge at the time of the invention to use signals received on a package pin of the processor for interrupts. The advantage of using processor pins for interrupts is to input external interrupts to the processor since the pins are the only means of communication in a typical processor.

32. As to claim 48, any pin with the functionality recited in claim 47 could be considered a SMI# package pin. The terminology makes no difference.

33. As to claim 49, Examiner asserts that it was common knowledge at the time of the invention to use an APIC bus for receiving interrupts. The advantage of using an APIC bus for interrupts is to allow external interrupts be efficiently transferred to a processor.

34. As to claim 50, Examiner asserts that it was common knowledge at the time of the invention to use a front side bus for receiving interrupts. The advantage of using a front side bus for interrupts is to allow external interrupts be efficiently transferred to a processor.

35. As to claims 51-53, Examiner asserts that it was common knowledge at the time of the invention to send interrupts from the Northbridge and Southbridge controller (both are processor chips). The advantage of sending interrupts from Northbridge and Southbridge controllers is to allow external hardware to interrupt the processor.

36. As to claim 56, Examiner asserts that it was common knowledge at the time of the invention to upon completion of an interrupt, changing the contents of a hardware register indicating the cause of the interrupt. One advantage of

indicating the cause of the interrupt is to add debug information for executing code.

37. Claims 36-42 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wooten'299 in view of Russell and in further view of common knowledge in the art.

38. Claims 36-42 and 45 recite equivalent limitations as claims 47-53 and 56. The claims are rejected for the same reasons.

Allowable Subject Matter

39. Claims 1-4, 26, 27 and 29-34 are allowed.

Response to Arguments

40. Applicant's arguments with respect to claims 1-17 and 29-34 have been fully considered and are persuasive. The rejection of these claims under 35 USC 102 has been withdrawn.

41. Applicant's arguments have been fully considered but they are not persuasive.

Regarding the arguments directed to claim 18, Examiner disagrees. The claim merely states that the instructions **allow** execution. Inherently, in an x86 processor, all of these claimed limitations are possible. Even though Wooten does not explicitly disclose performing these actions. Any code running on the system would make these actions possible

42. Applicant states:

> Russell is directed to a method of managing time between multiple protected mode execution environments. (Col. 2, lines 40-45). To switch between modes, Russell describes a "context register" to indicate which execution environment is active. (Col. 8, lines 55-62). The Examiner argues that the context register of Russell is a global descriptor table register. (Office Action, Page 8). A global descriptor table register holds the base address of a global descriptor table (See e.g., page 11-6 of the Pentium Processor User's Manual, Volume 3: Architecture and Programming Manual), whereas Russell's context register simply indicates which execution environment is active. (Col. 6, lines 39-43; Col. 7, lines 22-25). Moreover, even though Russell discloses that each execution environment contains a global descriptor table register, Russell fails to teach or suggest the claimed approach of "replacing first contents of the global descriptor register that point to a first global descriptor table in use when the system management mode interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table" as recited by independent claims 1 and 5. For at least this reason, it is clear that Wooten and Russell, individually and in combination, fail to teach or suggest the claimed invention.

Examiner disagrees. As stated, the context register points to a pointer to the table. Therefore, it indirectly points to the table. When the mode is changed, the register would therefore point to a new table as claimed.

43. Applicant states:

> In addition, with regard to dependent claims 34 and 44, the Examiner asserts that VSM returns by any means for returning from the SMI. (Office Action, Pages 12 and 6). However, Wooten fails to teach or suggest "returning from the interrupt by executing an RSM instruction" as recited by claims 34 and 44. In fact, exiting in such a manner is incompatible with VSM because Wooten describes only three instructions to exit VSM: IRET, RECC, and RENCC. (Col. 3, lines 24-27; Col. 18, lines 28-32). Because Wooten does not describe exiting VSM by executing an

> RSM instruction as recited by claims and 44, applicant respectfully requests that the Examiner reconsider and withdraw the rejection with regard to claims 34 and 44.

Examiner disagrees. The IREST, RECC, and RENCC instructions are considered to be RSM instructions. No further limitations for an RSM instruction are claimed.

44. Applicant states:

> "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." (MPEP § 2141.02(VI); emphasis in original). Consequently, a proper rejection cannot simply pick and choose particular elements from Wooten and Russell to find independent claims 1 and 5 unpatentable. It is improper to modify Wooten to arrive at the claimed invention because Wooten teaches away from the claimed invention. Specifically, Wooten teaches away from the claimed invention because Wooten defines a new mode of the processor-- VSM--which is not SMM.
>
> Indeed, not only does Wooten define VSM as a new mode, but Wooten also recommends against using SMM. For example, Wooten explains that "[i]n a 386 compatible processor, addressing mechanisms of a processor cannot be mixed between different modes of operation," which "complicates device emulation when using SMM because the SMM code must devote significant amounts of time in an address translation process." (Col. 2, lines 49-67). In fact, Wooten further explains that an "addressing mode change in SMM further exacerbates the overhead problems so that the use of the SMI is not readily feasible." (Col. 2, line 67 - Col. 3, line 2; emphasis added). Because VSM is clearly not SMM, and entering SMM is required by applicant's claims, Wooten teaches away from the claimed invention and it is improper to modify Wooten to render applicant's claims obvious.

Examiner disagrees. Wooten is merely pointing out shortcomings of previous SMM implementations. Similarly, the Applicant's invention does not perform exactly as other SMM implementations, but this does not make Applicant's SMM not a system management mode.

45. Regarding the rejection of claims 47-53, Examiner disagrees. The rejection modifies the VSM of Wooten in order to be able to use these methods

of changing modes. Examiner asserts that these methods were extremely well known in the art and it would have been obvious to **modify** the system of Wooten to use these methods. Applicant states that it is "impossible" to enter VSM mode using the recited mechanisms. Examiner requests that this be explained further. It would be fairly easy to implement an interrupt to run code to change system modes (into VSM) using an external interrupt. Additionally, Applicant admits that "Likewise, because one having ordinary skill in the art at the time the application was filed would have known that a front side bus connects the processor and chipset (See e.g., page 5 of Intel® 810E Chipset: Great Performance for All PCs, Revision 1.3, January 2001; attached herein), applicant's specification supports receiving a message via a front side bus (claims 29, 39, and 50)." Applicant's argument stating that the claims are enabled by the specification also show that Applicant believes that the limitations are also well known.

Conclusion

46. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 12/3/2007

ALFORD KINDRED
SUPERVISORY PATENT EXAMINER